REMARKS

In accordance with the foregoing, claims 17 and 18 have been amended and claims 35-37 have been cancelled. Claim 13 and 16-34 are pending, and claims 17-19, 23, 29 and 32 are currently under consideration. Because claim 17 is generic to the first through ninth species, the non-elected species claims have been allowed to remain pending.

Claim 18 is rejected under 35 USC § 102(a) or (e) as being anticipated by U.S. Patent Publication No. 2001/0001292 to Bertin et al. Although claim 18 is rejected, in the Examiner's description of the rejection he refers to the limitations of claim 17. Accordingly, it appears that the Examiner intended to reject claim 17 instead of claim 18. The rejection is defective because of this discrepancy.

The Examiner states that Bertin et al. discloses a semiconductor device, which includes: a semiconductor element substrate (chip) 15 (Fig. 20), a passive component (decoupling capacitor 136), mounted on the semiconductor element substrate 15, column-shaped conductors (chip-to-chip connectors 40A) formed on the semiconductor element substrate 15, and an insulation layer 101/103/105 burying the passive component and the column-shaped conductors 48. For the insulation layer, the Examiner refers to Fig. 10 and paragraph 50 of Bertin et al.

Layers 101/103/105 cited by the Examiner are sacrificial insulation layers existing over the semiconductor element substrate. However, referring to the first sentence in paragraph 50, Fig. 10 illustrates an example of the fabrication of chip-to-chip connectors 40. Fig. 10 simply shows one step in a fabrication process. The different sacrificial layers 101/103/105 are used to form different sized chip-to-chip connectors 40A and 40B. Referring to the last sentence in paragraph 50, all sacrificial insulating layers 101/103/105 are removed, with dielectric layer 97, or optionally dielectric layer 95 acting as an etch stop. An etch stop is required because further processing may be performed. Referring to Fig. 20, none of the sacrificial layers 101/103/105 are present in the final product.

Each of independent claims 17 and 18 requires a passive component. The Examiner has cited the decoupling capacitors 136 shown in Fig. 20 for this limitation. There is no suggestion in Bertin et al. that the decoupling capacitors 136 are ever present before the sacrificial layers 101/103/105 were removed. Claims 17 and 18 also require that the passive component be electrically connected to electrodes of the semiconductor element substrate. Even if the decoupling capacitors 136 of Fig. 20 were present together with the sacrificial layers 101/103/105, there is certainly no suggestion in Bertin et al. that the electrical connections are

made prior to the Fig. 10 process. Other electrical connections are not shown in Fig. 10.

Independent claim 18 recites an insulation layer burying a passive component and column-shaped conductors, which are formed over a semiconductor element substrate. Bertin et al. has no such insulation layer. Accordingly, Bertin et al. cannot achieve any of the significant benefits which may be associated with such an insulation layer. For example, since the passive component and the column-shaped conductors are buried in the insulation layer, any electrodes of the passive component and inter connections of the semiconductor element substrate may be protected from moisture by the insulation layer. Therefore, it may be possible to prevent any electrodes of the passive component and inter connections of the semicondcutor element substrate from corroding due to moisture condensation. Further, it may be possible to prevent any electrodes of the passive components and the inner connections of the semiconductor element substrate from being short-circuited.

The other references, such as U.S. Patent No. 5,986,301 to Fukushima et al., do not compensate for the deficiencies in Bertin et al. Accordingly, the rejection (assuming it was proper) should be withdrawn.

Claims 17, 19, 23, 29 and 32 are rejected under 35 USC § 103(a) as being obvious over Bertin et al. "in view of skill of ordinary person." On page 4 of the Office Action, the Examiner admits that Bertin et al. does not disclose column-shaped conductors having a height which is substantially flush with at least the upper surface of the passive component. To address this deficiency, the Examiner cites Fig. 19 of Bertin et al.,

In addition to the height requirement, independent claim 17 also recites an insulation layer burying the passive component and the column-shaped conductors. As described above, in the Fig. 20 product of Bertin et al., the sacrificial layer 101/103/105 is not present over the semiconductor element substrate 15. Likewise, Fig. 19 does not include the sacrificial layers 101/103/105.

Because Bertin et al. does not have an insulation layer as claimed, Bertin et al. cannot achieve any of the significant benefits which may be associated with such an insulation layer. For example, since the passive component and the column-shaped conductors are buried in the insulation layer, any electrodes of the passive component and inter connections of the semiconductor element substrate may be protected from moisture by the insulation layer. Therefore, it may be possible to prevent any electrodes of the passive component and inter connections of the semicondcutor element substrate from corroding due to moisture condensation. Further, it may be possible to prevent any electrodes of the passive components

and the inner connections of the semiconductor element substrate from being short-circuited.

The other references, such as U.S. Patent No. 5,986,301 to Fukushima et al., do not compensate for the deficiencies in Bertin et al. Accordingly, the rejection should be withdrawn.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: Sept. 1, 2004

By: M. Henry
Mark J. Henry
Registration No. 36,162

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

CERTIFICATE UNDER 37 CFR 1.8(a)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
on Sept. 1, 2004
STAAS & HALSEY
By: M. Henry
Date: 9.1.04